What is claimed is:

1. An apparatus comprising:

a pixel including (i) a buffer transistor having an input, (ii) first and second capacitive storage elements each of which selectively can be coupled to the input of the buffer transistor, and (iii) a photosensitive element having an output which selectively can be coupled to the input of the buffer transistor; and

a readout circuit that selectively can be coupled to an output of the buffer transistor.

2. The apparatus of claim 1 including:

a first switch coupled between the output of the photosensitive element and the input of the buffer transistor;

a second switch coupled between the first capacitive storage element and the input of the buffer transistor; and

a third switch coupled between the second capacitive storage element and the input of the buffer transistor,

each of the switches being selectively operable in an open or closed state.

3. The apparatus of claim 2 including a fourth switch coupled between a power supply node and the input of the buffer transistor, the fourth switch being selectively operable in an open or closed state.

4. The apparatus of claim 3 including a controller for providing signals to control the respective states of the first, second, third and fourth switches.

5. The apparatus of claim 4 wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time.

6. The apparatus of claim 5 wherein the controller is configured for providing signals to cause (i) the first and second switches to be closed during the first integration time, (ii) the third and fourth switches to be open during the first integration time, (iii) the first and third switches to be closed during the second integration time, and (iv) the second and fourth switches to be open during the second integration time.

7. The apparatus of claim 6 wherein the controller is configured for providing signals to cause (i) the first, second and fourth switches to be closed just prior to the first integration period, and (ii) the first, third and fourth switches to be closed just prior to the second integration period.

8. The apparatus of claim 6 wherein the controller is configured for providing signals to reset the photosensitive element and the first capacitive storage element prior to the first integration period and to reset the photosensitive element and the second capacitive storage element prior to the second integration period.

9. The apparatus of claim 5 wherein the controller is configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive element to the readout circuit.

10. The apparatus of claim 9 wherein the controller is configured for providing signals to reset the input of the buffer transistor prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to reset the input of the buffer transistor prior to transferring the second signal level from the second capacitive storage element to the readout circuit.

11. The apparatus of claim 9 wherein the controller is configured for providing signals to cause the fourth switch to be closed prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to cause the fourth switch to be closed just prior to transferring the second signal level from the second capacitive storage element to the readout circuit.

12. The apparatus of claim 3 wherein the fourth switch is configured for operation in a sub-threshold reset mode.

13. An integrated circuit comprising:

an array of pixels each of which is associated with a respective row and column in the array, each pixel including (i) a buffer transistor having an input, (ii) first and second capacitive storage elements each of which selectively can be coupled to the input of the buffer transistor, and (iii) a photosensitive element having an output which selectively can be coupled to the input of the buffer transistor;

readout circuitry which selectively can be coupled to outputs of buffer transistors of selected pixels in the array; and

a controller for providing signals to control the selective coupling of the first and second capacitive storage elements and the photosensitive element to the input of the

buffer and to control the selective coupling of the readout circuitry to the outputs of the buffer transistors.

14. The integrated circuit of claim 13, each pixel including:

a first switch coupled between the output of the photosensitive element and the input of the buffer transistor;

a second switch coupled between the first capacitive storage element and the input of the buffer transistor; and

a third switch coupled between the second capacitive storage element and the input of the buffer transistor,

each of the switches being selectively operable in an open or closed state.

15. The integrated circuit of claim 14, each pixel including a fourth switch coupled between a power supply node and the input of the buffer transistor, the fourth switch being selectively operable in an open or closed state.

16. The integrated circuit of claim 15 wherein the controller is configured for providing signals to control the respective states of the first, second, third and fourth switches.

17. The integrated circuit of claim 16 wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time.

18. The integrated circuit of claim 17 wherein the controller is configured for providing signals to cause (i) the first and second switches to be closed during the first integration time, (ii) the third and fourth switches to be open during the first integration time, (iii) the first and third switches to be closed during the second integration time, and (iv) the second and fourth switches to be open during the second integration time.

19. The integrated circuit of claim 18 wherein the controller is configured for providing signals to cause (i) the first, second and fourth switches to be closed just prior to the first integration period, and (ii) the first, third and fourth switches to be closed just prior to the second integration period.

20. The integrated circuit of claim 18 wherein the controller is configured for providing signals to reset the photosensitive element and the first capacitive storage element prior to the first integration period and to reset the photosensitive element and the second capacitive storage element prior to the second integration period.

21. The integrated circuit of claim 17 wherein the controller is configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuitry and to transfer the second signal level from the second capacitive element to the readout circuitry.

22. The integrated circuit of claim 21 wherein the controller is configured for providing signals to reset the input of the buffer transistor prior to transferring the first signal level from the first capacitive storage element to the readout circuitry and to reset the input of the buffer transistor prior to transferring the second signal level from the second capacitive storage element to the readout circuitry.

23. The integrated circuit of claim 21 wherein the controller is configured for providing signals to cause the fourth switch to be closed prior to transferring the first signal level from the first capacitive storage element to the readout circuitry and to cause the fourth switch to be closed just prior to transferring the second signal level from the second capacitive storage element to the readout circuitry.

24. The integrated circuit of claim 15 wherein the fourth switch is configured for operation in a sub-threshold reset mode.

25. A method comprising:

storing a first signal level, sensed by a photosensitive element, in a first capacitive storage element in a pixel;

storing a second signal level, sensed by the photosensitive element, in a second capacitive storage element in the pixel; and

reading out the first and second signal levels from the pixel.

26. The method of claim 25 including obtaining a signal representing the difference between the first and second signal levels read from the pixel.

27. The method of claim 25 wherein the first signal level is stored during a first integration period and the second signal level is stored during a second integration period.

28. The method of claim 27 including:

resetting the photosensitive element and the first capacitive storage element prior to the first integration period; and

resetting the photosensitive element and the second capacitive storage element prior to the second integration period.

29. The method of claim 28 including reading out the first and second signal levels from the pixel through a buffer transistor, the method further including:

resetting an input of the buffer transistor prior to reading out the first signal level from the first capacitive storage element; and

resetting the input of the buffer transistor prior to reading out the second signal level from the second capacitive storage element.

30. The method of claim 28 including operating a pixel reset switch in a sub-threshold reset mode.